Dr. Sudhakar S. Mande
Professor and Head of Department
Don Bosco Institute of Technology,
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Educational Qualification

PhD (Microelectronics) from IIT Bombay in June 2011
M.Tech (Microelectronics) with CPI of 8.66 from IIT Bombay in January 2000.
B.E. (Electronics) with Distinction from Marathawada University in August 1992.

M.Tech project Work

"**Lateral Asymmetric Channel (LAC) MOSFETs for ULSI Applications**"

In this work a novel technique is developed for the extraction of channel length for 100nm LAC and Convention MOSFETs. This technique combines a well-known Shift & Ratio technique and Charge Pumping Technique. With help of experimental result suitability of 100nm LAC MOSFET for high speed low power ULSI applications is verified.

PhD Research Work

"Variability Aware Performance Evaluation of Nanoscale CMOS Devices and Circuits"

My research work addresses the issue of increased level of process variations and consequent yield loss in nanoscale CMOS Integrated Circuits. To address this issue, a novel approach to generate process variation aware compact models is developed. Such compact models capture the variations in significant process parameters and translate these variations to circuit performance using Industry standard circuit simulators like SPICE or SPECTRE. Our approach combines well-known Statistical methods like Plackett-Burman Design of Experiment (PB-DOE) method, Response Surface Methodology (RSM), and Principal Component Analysis (PCA). The validity of the proposed approach is confirmed against TCAD simulator for identical process conditions. In this work, PB-DOE method is also explored for variability aware dual-Vth assignment for low power nanoscale CMOS design.

Software skills

· Operating System such as DOS, WINDOWS and LINUX
· Programming Languages such as 'C' and BASIC
· VLSI Design Softwares Such as Spice, Magic, IRSIM

· TCAD tools such as Sprocess, Sdevice

Paper Published

[1] Sudhakar Mande and A.N.Chandorkar , "Response Surface Methodology for statistical characterization of nanoscale CMOS devices and Circuits," *in Proceedings of International Workshop on Physics of Semiconductor Devices*, Dec 2007, pp.297-300.
[2] A.N.Chandorkar, Sudhakar Mande and Hiroshi Iwai,"Estimation of Process Variation impact on DG-FinFET using Plackett-Burman Design Experiemt method," *in Proceedings of International Conference on Solid-State and Integrated-Circuit Technology*, Oct 2008, pp. 215-218.
[3] A.M.Chopade, R.A.Takker, Sudhakar Mande, M.B.Patil and A.N.Chandorkar, "Verification of Parameter Extraction Strategy for MOS Model 11," *in Proceedings of International Conference on Trends in Intelligent Electronic Systems*, (TIES 2007) Sathyabama University, Jeppiaar Nagar, Chennai, India.
[4] **Sudhakar Mande, A.N.Chandorkar, Cheng Hsaio, Kasa Huang, Y.M.Sheu and Sally Liu, "A Novel Approach to Link Process parameters to BSIM model Parameters," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 4, pp. 544-551, Nov. 2009.**
[5] **Sudhakar Mande, A. N. Chandorkar, Sourabh Chandorkar, " Process Variation Aware dual-Vth Approach for Low Power Design of Nanoscale CMOS Circuits," publication in Elseviers Journal of Microelectronics Reliability, August 2011.**
[6] T.Sing,J.Chacko,N.Sebastian, R. Thoppilan, A.Kotrashetti, S.Mande, "Design and optimization of microstrip Hairpin-Line bandpass filter using DOE methodology," International Conference on Communication, Information & Computing Technology (ICCICT), 2012.
[7] Sudhakar Mande, A.N.Chandorka and Hiroshi Iwai, "Computationally Efficient Methodology for Statistical Characterization of Inter- and Intra-die Process variations," *Asia Symposium on Quality Electronic Design*, Dec 2013, pp.287-294.
[8]Hansel Dsilva, Julian Pinto, Arzhan Elchidana and Sudhakar Mande, "Variability aware performance evaluation of low power SRAM cell", *Asia Symposium on Quality Electronic Design*, Dec 2013, pp.183-187.
[9] Mahesh Kadam, Kishor Sawarkar, and Sudhakar Mande, "Comparative analysis and efficient VLSI implementation of FIR filter" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue-7, July 2015.
[10] Mahesh Kadam, Kishor Sawarkar, and Sudhakar Mande, "Investigation of Suitable DSP Architecture for Efficient FPGA Implementation of FIR Filter", International Conference on Communication, Information and Computing Technology, 2015, Pages:1-4.
[11] Mohd Iqbal and Sudhakar Mande, "A Novel Successive Approximation Register ADC with Variable Conversion Time", IEEE International Advance Computing Conference, Andhra Pradesh, February 2016.

Invited Talks

1. MOSFET Basics and Scaling, July 2007, STTP, Terna Engineering College, Nerul, Navi Mumbai.
2. VLSI Design using WinSPICE, Nov 2008, STTP, Don Bosco Institute of Technology, Kurla, Mumbai.

3. Electronic Circuit Simulation using SPICE, STTP, KC College of Engineering, Thane, Jan 2009.
4. Modern Electronic Design Techniques using WinSpice, Feb 2009, RGIT, Mumbai.
5. Analog Circuit Design, STTP Saraswati Engineering College, Kharghar, Navi Mumbai, July 2009.
6. Optimization of Transistor Performance for VLSI Applications, Tasgaokar College of Engineering, Karjat, Thane, April 2010.
7. Integrated Circuit Design using WinSPICE, Pooranmal Lahoti Government Polytechique College, Latur, 23rd Jan 2011.
8. How to write a technical paper, Don Bosco Institute of Technology, DBIT-IEEE Chapter, September 2011
9. "Role of Electronics & Telecommunication Engineers in 21st Century, Yadavrao Tasgonakar College of Engineering and Technology, Bhivpuri, Karat. October 2011.
10. "Low Power VLSI Design," STTP, Lokmanya Tilak College of Engineering, Kopar Khairne, Navi Mumbai, 11th January 2012.
11. "Variability Aware Performance Evaluation of Nanoscale CMOS Devices and Circuits" 10 March 2012, Technical Talk Delivered to DBIT faculty members as part of Staff Development Programme.
12. "Past, Present, and Future of VLSI", Yadvarao Tasgaonkar Institute of Technology, Bhivpuri Road, Karjat, Thane, on 10 April 2012.
13. "Optimization of Signal Processing Algorithms for Efficient Implementation of VLSI Architectures", STTP on Advances in Signal Processing, KIT, Kholapur, 4 January 2013.
14. "Journeying from Electronics to Nanoelectronics", K. J. Somaiya Institute of Information Technology, Sion, Mumbai, 7 February 2013.
15. "Advanced Low Power VLSI Design" Fr. Angel College of Engineering, Vashi, Navi Mumbai, July 2013.
16. "In Search of research" Don Bosco Institute of Technology, Faculty Development Programme, January 10, 2014.
17. "CMOS Analog VLSI Design", Sandipani Institute of Technology, Nashik, February 2014.
18. "How Write Project Report" K K Wagh College of Engineering, Nashik, May 2014.
19. "Variability Aware Low Power Design of Nanoscale CMOS circuits", Saradar Patel Institute of Technology, Andheri(W), Mumbai, May 7, 2015
20. "Design of nanoscale Analog and Mixed Signal VLSI Design", Gujarath Technical University, Research Symposium, April 2015.
21. "VLSI Design: Road Map to Explore IoT and Multidimensional Opportunities", K.C. College of Engineering on September 22, 2015.
22. "Design of MOS Differential Amplifier and two stage Operation Amplifier", Sardar Pater Institute of Technology on December 9, 2015.
23. "Statistical Techniques for the performance evaluation of Nanoscale COS devices and Circuits", Gujrat Technical University on April 12, 2016.
24. "Nanoscale Low Power VLSI Design" Shah &Anchor College of Engineering, Chembur, Mumbai on July 1, 2016.

25. "Low Power VLSI Design", MIT College of Engineering, Kothrud, Pune on July 4, 2016.
26. "Electronics:Past, Present and Future," IEEE-WIE Outreach programme, DBIT on August 3, 2016.
27. "Nanoscale Low Power Design using Design of Experiment Technique", Harne College of Engineering, B.R. Harne College of Engineering, Badlapur, on August 6, 2016.
28. "Workshop of Next Generation Simulation Programme with Integrated Circuit Empasis (Ngspice)," KC College of Engineering, Thane on December 19-20, 2016.

Number of M.E students guided 2.
Two PhD students registered in University of Mumbai under my supervision.

Professional Membership

IETE Fellow, ISTE Life Membership, IEEE Member

Additional Responsibilities

- Member Board of Studies for Electronic and Telecommunication Engineering, University of Mumbai since November 2012-March 2016.
- Member of Academic Advisory Board for Electronics & Telecommunication Engineering in Rajiv Gandhi Institute of Technology, Panel member for the evaluation of PhD and M.Tech thesis in **Gujrath Technical University, Ahemdabad.**
- Working as Chairman of Board of Studies of Electronics Engineering in University of Mumbai since April 2016.
- Working as Chairman of IETE Navi Mumbai Centre since July 2016.
- Member of Department Advisory Board for Electronics and Telecommunication Engineering in Fr. Agnel College of Engineering, Vashi, Navi Mumbai.

Work Experience

1. Worked as a Lecturer in Department of Electronics and Telecommunication in MGM's College of Engineering and Technology, Kamothe, Navi Mumbai since 9th September 1992 to 31st August 2002.
2. Worked as an Assistant Professor in Department of Information Technology in MGM's College of Engineering and Technology, Kamothe, Navi Mumbai since 1st September 2002 to 30 June 2004.
3. Worked as Head of the Department of Electronics & Telecommunication in MGM's College of Engineering and Technology, Kamothe, Navi Mumbai since 1st July 2001 to June 2002.
4. Worked as Management Representative for ISO Certification in MGM's College of Engineering and Technology, Kamothe, Navi Mumbai

5. Worked as Assistant Professor in Department of Electronics & Telecommunication Engineering in Don Bosco Institute of Technology since July 1, 2004 to June 30, 2011
6. Worked as Associate Professor in Department of Electronics & Telecommunication Engineering in Don Bosco Institute of Technology since July 1, 2011 to June 30, 2015.
7. Worked as Member of Board of studies for Electronics & Telecommunication Engineering from November 2013 to November 2015.
8. Worked as Publication Chair for International Conference on Technologies for Sustainable Development 2015.
9. Working as Professor in Department of Electronics and Telecommunication Engineering of Don Bosco Institute of Technology, Mumbai from July 1, 2015.
10. Working as **Head of Department** of Electronics & Telecommunication Engineering in Don Bosco Institute of Technology since July 1, 2014 to till date.